Sub A2

ABSTRACT

The present invention is defined in that an information processing device which reads, buffers, decodes and executes instructions from an instruction store portion by pipeline processing comprises: an instruction reading request portion which assigns a read address to the instruction store portion; an instruction buffering portion including a plurality of instruction buffers which buffer an instruction sequence read from the instruction store portion; an instruction execution unit which decodes and executes instructions buffered by the instruction buffering portion; a branching instruction detection portion which detects a branching instruction in the instruction sequence read from the instruction store portion; and a branch target address information buffering portion including a plurality of branch target address information buffers which, when the branching instruction detection portion has detected a branching instruction, buffer the branch target address information for generating the branch target address of the branching instruction; wherein, when the branching instruction detection portion has detected a branching instruction, either the branch target address information of the branching instruction is stored in one of the plurality of branch target address information buffers, or the branch target instruction sequence of the branching instruction is stored in one of the plurality of instruction buffers in addition to the

storing in the branch target address information buffer.